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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/656,013	09/05/2003	Subhasish Mitra	ITL.0971US (P16171)	8151

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EXAMINER	
CHUNG, PHUNG M	

ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
10/31/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/656,013	MITRA ET AL.	
	Examiner	Art Unit	
	Phung My Chung	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *03 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 101

1. 35 U.S.C. 101 reads as follows:

> Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

2. Claims 1-25 are rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

The claims merely recite a series of mathematical operation or calculations (i.e. mathematical algorithms) by reciting the following steps of:

Adding at least two columns to a compactor matrix...;

Obtaining the maximum number...;

Reducing the compactor matrix...'

Eliminating...;

Adding values to the matrix rows...; and

Obtaining a number of circuit outputs...

Thus, the claimed invention does nothing other than present and solves a series of mathematical operations. Therefore, claims 1-25 are not patentable under 35 U.S.C. 101.

Claim Rejections - 35 USC § 112

3. Claims 1-25 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 1, lines 1-3, the claim as a whole is not under stood. What is meant by "adding at least two columns to a compactor matrix for each circuit output that, at the same time, produce an unknown logic value? What is the result of adding, what it is for? How it is related to the unknown logic value?

As per claim 2, lines 1-2, "adding at least two columns...at the same time" is not clear as to what it meant. What is the result of adding and what it is for? How it is related to the unknown logic values.

In addition, line 2, "can" a positive term should be used.

As per claim 3, this claim is also rejected because it dependent upon the rejected base claim.

As per claim 4, lines 1-3, "wherein adding at least one column...unknown logic value includes adding two columns...for each scan chain" the claim is not clear because the word "wherein" is referred to any step or means that is mentioned before and "includes adding two columns to the matrix for each such scan chain" this limitation already recited in claim 2. In addition, line 2, "can" a positive term should be used.

As per claim 5, lines 1-2, "reducing the compactor matrix using maximum compatibility class problem" what is meant by using maximum compatibility class problem?

As per claim 6, this claim is also rejected because it dependent upon the rejected base claim.

As per claim 7, line 1, "a compactor matrix" should be changed to - - the compactor matrix - -.

As per claim 8, this claim is also rejected because it dependent upon the rejected base claim.

As per claim 9, lines 5-6, "adding at least two columns...produce unknown logic values" is not clear what is the result of adding and what it is for? How it is related to unknown logic values.

As per claim 10, line 1, "a process" and "a number" should be changed to - - the process - - and - - the number - -; and line 2, "can" a positive term should be used.

As per claim 11, line 1, "a process" should be changed to - - the process - -;

Lines 2-4, "wherein adding at least one column...unknown logic value includes adding two columns...for each scan chain" the claim is not clear because the word "wherein" is referred to any step or means that is mentioned before and "includes adding two columns to the matrix for each such scan chain" this limitation already recited in claim 9. In addition, line 2, "can" a positive term should be used.

As per claim 12, this claim is also rejected because it dependent upon the rejected base claim.

As per claim 13, line 1, "a process" should be changed to - - the process - -;

As per claim 14, line 1, "a process" should be changed to - - the process - - ;

Line 2, "a compactor matrix" should be changed to - - the compactor matrix - -;

and Line 3, "can" a positive term should be used.

As per claim 15, line 1, "a process" should be changed to - - the process - -.

As per claim 16, lines 1-3, "a response compactor...to handle any number of scan chains with unknown logic values" the claim as a whole is not under stood. It is

not clear how the exclusive OR gates are coupled (parallel or series?) and how they handled any number of scan chains with unknown logic values?

As per claim 17, lines 1-2, "to handle any number of errors in the same scan cycle" is not clear how they handle any number of errors in the same scan cycle.

As per claim 18, this claim is also rejected because it dependent upon the rejected base claim.

As per claim 19, lines 3-4, "add at least two columns to a compactor matrix...produce an unknown logic value" What is meant by "add at least two columns to a compactor matrix for each circuit output that, at the same time, produce an unknown logic value? What is the result of adding, what it is for? And how it is related to the unknown logic value?

As per claim 20, line 2, "a processor-based system" should be changed to - - the processor-based system - -; and

Line 2, "can" a positive term should be used.

As per claim 21, lines 1-2, "a processor-based system" should be changed to - - the processor-based system - -.

As per claim 22, lines 1-2, "storing instruction that, if executed, enable the compactor matrix to be reduced using maximum compatibility class problem" is not clear as to what it meant.

As per claim 23, lines 1-2, ""a processor-based system" should be changed to - - the processor-based system - -.

As per claim 24, lines 1-2, "a processor-based system" should be changed to - - the processor-based system - -.

As per claim 25, lines 1-2, "a processor-based system" should be changed to - - the processor-based system - -.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

The changes made to 35 U.S.C. 102(e) by the American Inventors Protection Act of 1999 (AIPA) and the Intellectual Property and High Technology Technical Amendments Act of 2002 do not apply when the reference is a U.S. patent resulting directly or indirectly from an international application filed before November 29, 2000. Therefore, the prior art date of the reference is determined under 35 U.S.C. 102(e) prior to the amendment by the AIPA (pre-AIPA 35 U.S.C. 102(e)).

5. Claims 1-25, as best understood, are rejected under 35 U.S.C. 102(e) as being anticipated by Rajski et al (6,557,129).

As per claims 16-18, Rajski et al disclose a response compactor comprising:

A plurality of coupled exclusive OR gates (48) to handle any number of scan chains (44) with unknown logic values. (See abstract, Fig. 8, col. 5, lines 65-67 to col. 6, lines 1-6).

As per claims 1-15 and 19-25, these claims are rejected under similar rationale as set forth in claims 16-18.

6. Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 571-272-3818. The examiner can normally be reached on Monday to Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques can be reached on 571-272-6962. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a

USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Phung My Chung
Primary Patent Examiner
Art Unit 2117